UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/505,387	08/20/2004	Mario Engelmann	PC10373US	7211

7590 10/28/2009

Robert P Seitter
RatnerPrestia
One Westlakes, Berwyn, Suite 301
P O Box 980
Valley Forge, PA 19482-0980

EXAMINER	
MURALIDAR, RICHARD V	
ART UNIT	PAPER NUMBER
2858	

MAIL DATE	DELIVERY MODE
10/28/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/505,387	ENGELMANN ET AL.	
	Examiner	Art Unit	
	RICHARD V. MURALIDAR	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *remarks filed 6/23/2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13,14,16 and 19-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13,14,16 and 19-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the reply dated 6/23/2009. Claims 1-12, 15, and 17-18 have been cancelled by the applicant. Claims 13, 14, 16, and 19-29 are currently pending for examination.

2. In responding to this Office action, applicants are reminded of the requirements of 37 CFR 1.111 and 1.119 that applicants specifically point out the specific distinctions believed to render the claims patentable over the references in presenting responsive arguments. See MPEP 714.02. The support of any amendments made should also be specifically pointed out. See MPEP 2163.06.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. **Claims 13, 14, 16, and 19-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Frait [U.S. 4398252] in view of Furuya et al. [U.S. 6322166].**

6. With respect to independent claims13 and 29, Frait discloses a method for generating a corrected nominal current in a pulse-width-modulated current control, in particular for electronic brake control units of motor vehicles,

wherein a measured current [Fig. 4, current sensing resistor 40 and current sensing transistor 92] is determined at a certain predetermined time during an actuation period [col. 7 lines 2-5; lines 31-35] and a compensation is executed by way of at least one compensation current value determined in response to a supply voltage [col. 6 lines 5-9; col. 7 lines 50-60], the compensation current value being added to the measured current so that the corrected nominal current is available for current control [col. 5 lines 23-38; col. 6 lines 61-67; col. 7 lines 50-68 and col. 8 lines 1-5; Fig. 4, the current control signal from 40 and 92 is combined (added at the connecting nodes shown) with the voltage supply compensated signal at 58 and 61. A control signal based on this combination is then sent along output-line 75 to control the switching of main switch 39]. Claim 29 additionally positively recites a “valve”- see [Frait, Abstract].

7. It is clear that Frait discloses that the compensation current value is *added to/adjusted with* the measured current value, to produce the final control signal (as described above). However, where this interpretation does not meet the limitation as applicant intended; Furuya discloses a PWM controlled brake system with supply voltage measurement and temperature measurement that are added to each other to

compensate the final control signal [see Furuya, col. 6 lines 49-67 and col. 7 lines 1-6; col. 7 lines 35-42; which states that these two values are added to each other].

8. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Furuya into Frait, for the benefit of utilizing a signal (itself comprising two added signals) to supply the final control signal for the benefit of efficiently combing two separate characteristics, each known to affect current through the coil- that being supply/battery voltage and measured current/temperature.

9. With respect to claim 14, Furuya discloses a method wherein the supply voltage dependency is compensated [col. 17 lines 60-67 and col. 18 lines 1-5].

10. With respect to claim 16, Furuya discloses a method wherein several loads are driven, and the compensation current value is fixed individually for each load, in particular for each valve coil [col. 8 lines 37-49; col. 11 lines 5-15; col. 15 lines 42-52].

11. With respect to claim 19, Furuya discloses a method wherein an averaging operation is executed by way of the present nominal value and previous nominal values to compensate abrupt changes in nominal values [col. 15 lines 60-67 and col. 16 lines 1-35].

12. With respect to claim 20, Furuya discloses a method wherein the temperature is determined indirectly by way of the Duty Cycle adjusted by current control [col. 18 lines 6-15].

13. With respect to claim 21, Furuya discloses a method wherein the sum of the coil resistor and the resistor of the connected semiconductor component for driving the load is taken into consideration for the determination of temperature [col. 18 lines 6-15,

the duty ratio from which temperature is determined is affected by both all resistances in the circuit, including the coil and the switch].

14. With respect to claim 22, Furuya discloses a method wherein the Duty Cycles of several PWM periods are averaged for temperature measurement or the determination of the indirect temperature value [the duty cycle of gradient z encodes the temperature information within in, col. 15 lines 60-67 and col. 16 lines 1-35].

15. With respect to claim 23, Furuya discloses a method wherein the nominal resistance value of the coil is used at the presently measured or estimated temperature of the control unit for the average value of the indirectly determined temperature quantity directly after the switching on of the ignition, in particular after the ignition's re-start [col. 14 lines 56-60; col. 19 lines 6-20].

16. With respect to claim 24, Furuya discloses a circuit arrangement for driving several inductive loads comprising a circuit for the PWM control of the load current, wherein the method as claimed in claim 13 is implemented as a program [Fig. 7, Fig. 9, Fig. 11, Fig. 16, Fig. 22, Fig. 25] in a microcomputer or microcomputer system [Fig. 1, control means] which is electrically connected to the PWM circuit.

17. With respect to claims 26-28, Furuya discloses a solenoid valve control circuit/method for use in electronic brake control units [col. 1 lines 5-19] wherein the compensation variables are stored in a table [col. 3 lines 59-64; col. 4 lines 1-20] and an interpolation is carried out for temperatures lying between two table values [Fig. 17, col. 18 lines 21-28] and supply voltages lying between two table values [col. 17 lines 3-6] in order to determine the compensation variable [Figs. 17, and 18; all points are

shown on all three curves Large, Medium, Small, for temperature and voltage for the range shown. One of ordinary skill in the art (first year engineering student) would certainly know how to interpolate/extrapolate a chart like this to find intervening values as well as values above or below the shown range. See Fig. 21 for discrete data points shown; where one of ordinary skill would find it useful to determine an interpolated value between, say, the **point A25C** and the point immediately below it, for the benefit of determining exactly what the current was doing at that fractional time increment

Response to Arguments

18. Applicant's arguments received 6/23/2009 have been considered but are unpersuasive. Applicant argues that Frait is missing, at least, the “added” portion of the limitation of claim 1. As explained in the action, the “added” limitation is construed to mean *combined*, and is given by Frait in col. 5 lines 23-38; col. 6 lines 61-67; col. 7 lines 50-68 and col. 8 lines 1-5; Fig. 4. The current control signal from 40 and 92 is combined (added at the connecting nodes shown) with the voltage supply compensated signal at 58 and 61. A control signal based on this combination is then sent along output-line 75 to control the switching of main switch 39. This interpretation is reasonable because the applicant has not recited control circuitry that arithmetically adds signals together. Even if one were to construe "added” narrowly, it is the examiner’s understanding that Furuya discloses this narrower interpretation of adding supply voltage measurement and temperature measurement to each other to compensate the final control signal [see Furuya, col. 6 lines 49-67 and col. 7 lines 1-6; col. 7 lines 35-42]. Thus the examiner

remains unconvinced that, at least the combination of Frait and Furuya does not produce the claims are currently recited.

19. **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to RICHARD V. MURALIDAR whose telephone number is (571)272-8933. The examiner can normally be reached on 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick J. Assouad can be reached on 571-272-2210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Richard V Muralidar/
Examiner, Art Unit 2858

/Patrick J Assouad/
Supervisory Patent Examiner, Art Unit 2858